

Am2946/Am2947

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems; PNP inputs reduce input loading
- $V_{CC} - 1.15V_{OH}$ interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability; Low power - 8mA per bidirectional bit
- Am2946 inverting transceivers; Am2947 noninverting transceivers; Transmit/Receive and Chip Disable simplify control logic
- Bus port stays in hi-impedance state during power up/down

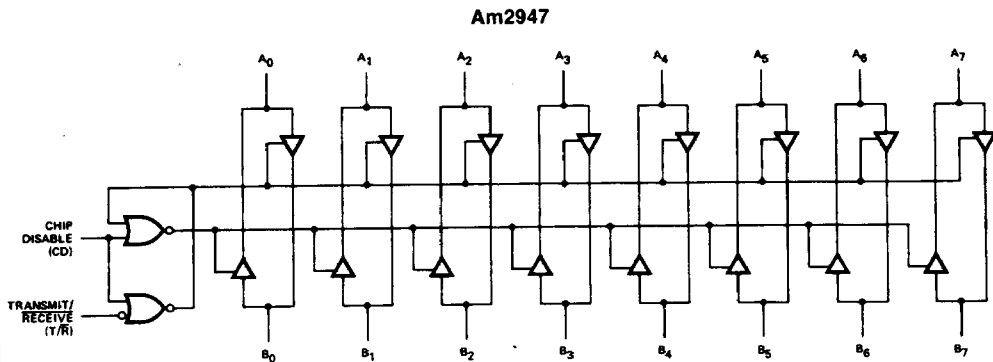
GENERAL DESCRIPTION

The Am2946 and Am2947 are 8-bit state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/Receive, determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (V_{OH}) is specified at $V_{CC} - 1.15V$ minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

BLOCK DIAGRAM

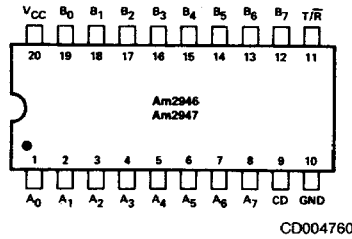


BD002530

Am2946 has inverting transceivers.

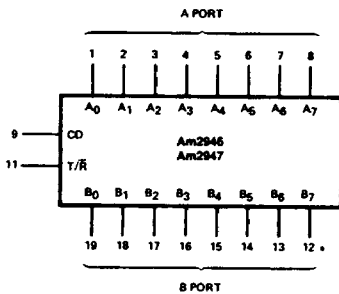
CONNECTION DIAGRAM Top View

D-20-1



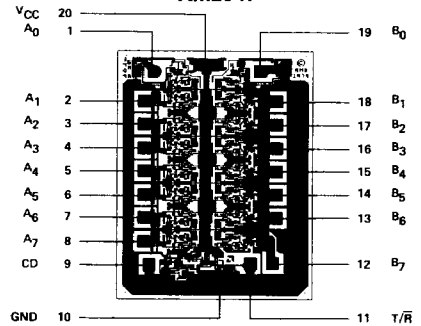
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS001060

METALLIZATION AND PAD LAYOUT Am2947

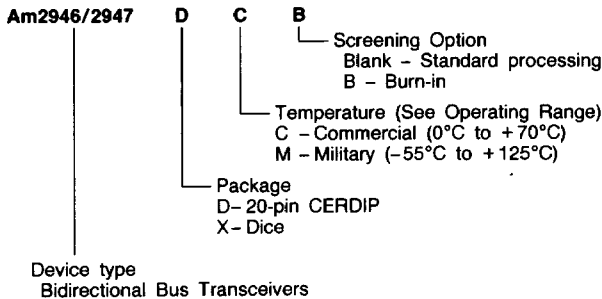


DIE SIZE .069" x .089"

Note: The Am2946 has inverting transceivers

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations

Am2946 Am2947	PC DC, DCB, DM, DMB XC
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Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A ₀ -A ₇	I/O	A port inputs/outputs are receiver output drivers when T/ \bar{R} is LOW and are transmit inputs when T/ \bar{R} is HIGH.
	B ₀ -B ₇	I/O	B port inputs/outputs are transmit output drivers when T/ \bar{R} is HIGH and receiver inputs when T/ \bar{R} is LOW.
9	CD	I	Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, \overline{CS}).
11	T/ \bar{R}	I	Transmit/Receive direction control determines whether A port or B port drivers are in 3-state. With T/ \bar{R} HIGH A port is the input and B port is the output. With T/ \bar{R} LOW A port is the output and B port is the input.

FUNCTION TABLE

Inputs	Conditions		
	L	L	H
Chip Disable	L	L	H
Transmit/Receive	L	H	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Solder, 10 seconds)	300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V

Military (M) Devices

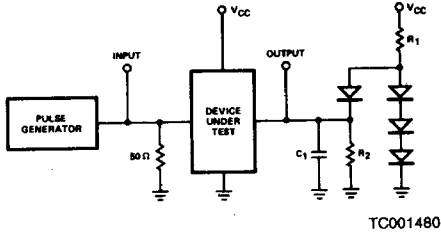
Temperature	-55°C to +125°C
Supply Voltage	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

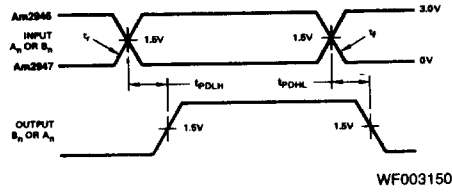
DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units	
A PORT (A₀-A₇)							
V _{IH}	Logical "1" Input Voltage	CD = V _{IH} MAX, T/ \bar{R} = 2.0V	2.0			Volts	
V _{IL}	Logical "0" Input Voltage	CD = V _{IL} MAX T/ \bar{R} = 2.0V	COM'L		0.8	Volts	
				MIL			0.7
V _{OH}	Logical "1" Output Voltage	CD = V _{IL} MAX, T/ \bar{R} = 0.8V	I _{OH} = -0.4mA I _{OH} = -3.0mA	V _{CC} - 1.15	V _{CC} - 0.7	Volts	
				2.7	3.95		
V _{OL}	Logical "0" Output Voltage	CD = V _{IL} MAX, T/ \bar{R} = 0.8V	I _{OL} = 12mA COM'L I _{OL} = 24mA		0.3	0.4	
					0.35	0.50	
I _{OS}	Output Short Circuit Current	CD = V _{IL} MAX, T/ \bar{R} = 0.8V, V _O = 0V, V _{CC} = MAX, Note 2	-10	-38	-75	mA	
I _{IH}	Logical "1" Input Current	CD = V _{IL} MAX, T/ \bar{R} = 2.0V, V _I = 2.7V		0.1	80	μ A	
I _I	Input Current at Maximum Input Voltage	CD = 2.0V, V _{CC} = MAX, V _I = V _{CC} MAX			1	mA	
I _{IL}	Logical "0" Input Current	CD = V _{IL} MAX, T/ \bar{R} = 2.0V, V _I = 0.4V		-70	-200	μ A	
V _C	Input Clamp Voltage	CD = 2.0V, I _{IN} = -12mA		-0.7	-1.5	Volts	
I _{OD}	Output/Input 3-State Current	CD = 2.0V	V _O = 0.4V V _O = 4.0V		-200	μ A	
					80		
B PORT (B₀-B₇)							
V _{IH}	Logical "1" Input Voltage	CD = V _{IL} MAX, T/ \bar{R} = V _{IL} MAX	2.0			Volts	
V _{IL}	Logical "0" Input Voltage	CD = V _{IL} MAX, T/ \bar{R} = V _{IL} MAX	COM'L		0.8	Volts	
				MIL			0.7
V _{OH}	Logical "1" Output Voltage	CD = V _{IL} MAX, T/ \bar{R} = 2.0V	I _{OH} = -0.4mA I _{OH} = -5.0mA I _{OH} = -10mA	V _{CC} - 1.15	V _{CC} - 0.8	Volts	
				2.7	3.9		
				2.4	3.6		
V _{OL}	Logical "0" Output Voltage	CD = V _{IL} MAX, T/ \bar{R} = 2.0V	I _{OL} = 20mA I _{OL} = 48mA		0.3	0.4	
					0.4	0.5	
I _{OS}	Output Short Circuit Current	CD = V _{IL} MAX, T/ \bar{R} = 2.0V, V _O = 0V, V _{CC} = MAX, Note 2	-25	-50	-150	mA	
I _{IH}	Logical "1" Input Current	CD = V _{IL} MAX, T/ \bar{R} = V _{IL} MAX, V _I = 2.7V		0.1	80	μ A	
I _I	Input Current at Minimum Input Voltage	CD = 2.0V, V _{CC} = MAX, V _I = V _{CC} MAX			1	mA	
I _{IL}	Logical "0" Input Current	CD = V _{IL} MAX, T/ \bar{R} = V _{IL} MAX, V _I = 0.4V		-70	-200	μ A	
V _C	Input Clamp Voltage	CD = 2.0V, I _{IN} = -12mA		-0.7	-1.5	Volts	
I _{CO}	Output/Input 3-State Current	CD = 2.0V	V _O = 0.4V V _O = 4.0V		-200	μ A	
					200		
CONTROL INPUTS CD, T/\bar{R}							
V _{IH}	Logical "1" Input Voltage		2.0			Volts	
V _{IL}	Logical "0" Input Voltage		COM'L		0.8	Volts	
				MIL			0.7
I _{IH}	Logical "1" Input Current	V _I = 2.7V		0.5	20	μ A	
I _I	Input Current at Maximum Input Voltage	V _{CC} = MAX, V _I = V _{CC} MAX			1.0	mA	
I _{IL}	Logical "0" Input Current	V _I = 0.4V	T/ \bar{R}	-0.1	-0.25	mA	
			CD	-0.1	-0.25		
V _C	Input Clamp Voltage	I _{IN} = -12mA		-0.8	-1.5	Volts	
POWER SUPPLY CURRENT							
I _{CC}	Power Supply Current	Am2946	CD = V _I = 2.0V, V _{CC} = MAX		70	100	mA
			CD = 0.4V, V _I = 2.0V, V _{CC} = MAX		100	150	
		Am2947B	CD = 2.0V, V _I = 0.4V, V _{CC} = MAX		70	100	
			CD = V _I = 0.4V, T/ \bar{R} = 2.0V, V _{CC} = MAX		90	140	

SWITCHING TEST CIRCUIT



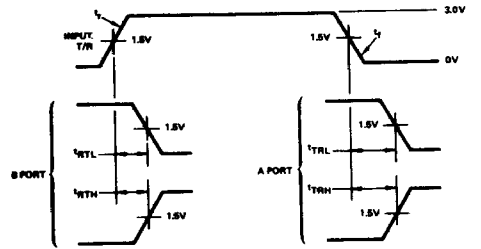
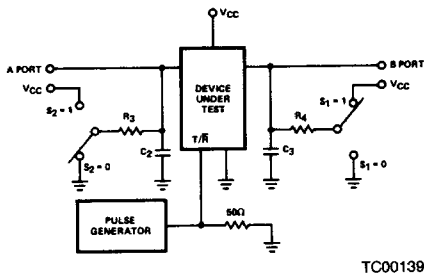
SWITCHING TIME WAVEFORM



Note: C_1 includes test fixture capacitance.

$$t_r = t_f < 10\text{ns } 10\% \text{ to } 90\%$$

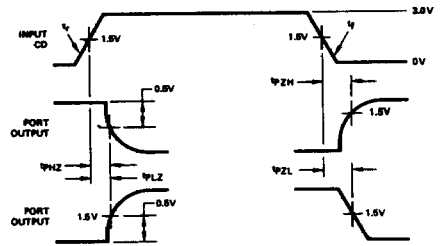
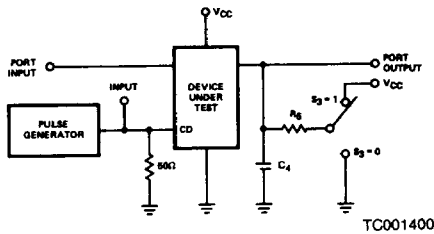
Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



Note: C_2 and C_3 include test fixture capacitance.

$$t_r = t_f < 10\text{ns } 10\% \text{ to } 90\%$$

Figure 2. Propagation Delay from T/R to A Port or B Port.



Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition.

$$t_r = t_f < 10\text{ns } 10\% \text{ to } 90\%$$

Figure 3. Propagation Delay from CD to A Port or B Port.

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)
Am2946

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
tpDHLA	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$, $R_2 = 5\text{k}$, $C_1 = 30\text{pF}$	8	12	ns
tpDLHA	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$, $R_2 = 5\text{k}$, $C_1 = 30\text{pF}$	11	16	ns
tpLZA	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to $B_7 = 2.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	10	15	ns
tpHZA	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to $B_7 = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	8	15	ns
tpZLA	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to $B_7 = 2.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 1\text{k}$, $C_4 = 30\text{pF}$	19	25	ns
tpZHA	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to $B_7 = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 5\text{k}$, $C_4 = 30\text{pF}$	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
tpDHLB	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$, $R_2 = 1\text{k}$, $C_1 = 300\text{pF}$	12	18	ns
		$R_1 = 667\Omega$, $R_2 = 5\text{k}$, $C_1 = 45\text{pF}$	7	12	ns
tpDLHB	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$, $R_2 = 1\text{k}$, $C_1 = 300\text{pF}$	15	20	ns
		$R_1 = 667\Omega$, $R_2 = 5\text{k}$, $C_1 = 45\text{pF}$	9	14	ns
tpLZB	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to $A_7 = 2.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	13	18	ns
tpHZB	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to $A_7 = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	8	15	ns
tpZLB	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to $A_7 = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 100\Omega$, $C_4 = 300\text{pF}$	25	35	ns
		$S_3 = 1$, $R_5 = 667\Omega$, $C_1 = 45\text{pF}$	16	22	ns
tpZHB	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to $A_7 = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 1\text{k}$, $C_4 = 300\text{pF}$	22	35	ns
		$S_3 = 0$, $R_5 = 5\text{k}$, $C_1 = 45\text{pF}$	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
tTRL	Propagation Delay from Transmit Mode to Receive a Logical "0", T/\bar{R} to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$, $R_4 = 100\Omega$, $C_3 = 5\text{pF}$ $S_2 = 1$, $R_3 = 1\text{k}$, $C_2 = 30\text{pF}$	23	33	ns
tTRH	Propagation Delay from Transmit Mode to Receive a Logical "1", T/\bar{R} to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 0$, $R_4 = 100\Omega$, $C_3 = 5\text{pF}$ $S_2 = 0$, $R_3 = 5\text{k}$, $C_2 = 30\text{pF}$	22	33	ns
tRTL	Propagation Delay from Transmit Mode to Receive a Logical "0", T/\bar{R} to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$, $R_4 = 100\Omega$, $C_3 = 300\text{pF}$ $S_2 = 1$, $R_3 = 300\Omega$, $C_2 = 5\text{pF}$	26	35	ns
tRTH	Propagation Delay from Transmit Mode to Receive a Logical "1", T/\bar{R} to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 0$, $R_4 = 1\text{k}$, $C_3 = 300\text{pF}$ $S_2 = 0$, $R_3 = 300\Omega$, $C_2 = 5\text{pF}$	27	35	ns

Note: 1. All typical values given are for $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
 2. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2946

Parameter	Description	Test Conditions	COMMERCIAL	MILITARY	Units
			Am2946	Am2946	
			Max	Max	
A PORT DATA/MODE SPECIFICATIONS					
t _{PDLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R ₁ = 1k, R ₂ = 5k, C ₁ = 30pF	16	19	ns
t _{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R ₁ = 1k, R ₂ = 5k, C ₁ = 30pF	20	23	ns
t _{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B ₀ to B ₇ = 2.4V, T/R = 0.4V (Figure 3) S ₃ = 1, R ₅ = 1k, C ₄ = 15pF	18	21	ns
t _{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B ₀ to B ₇ = 0.4V, T/R = 0.4V (Figure 3) S ₃ = 0, R ₅ = 1k, C ₄ = 15pF	18	21	ns
t _{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B ₀ to B ₇ = 2.4V, T/R = 0.4V (Figure 3) S ₃ = 1, R ₅ = 1k, C ₄ = 30pF	28	33	ns
t _{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B ₀ to B ₇ = 0.4V, T/R = 0.4V (Figure 3) S ₃ = 0, R ₅ = 5k, C ₄ = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t _{PDLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1)	24	29	ns
		R ₁ = 100Ω, R ₂ = 1k, C ₁ = 300pF R ₁ = 667Ω, R ₂ = 5k, C ₁ = 45pF	16	19	ns
t _{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1)	25	30	ns
		R ₁ = 100Ω, R ₂ = 1k, C ₁ = 300pF R ₁ = 367Ω, R ₂ = 5k, C ₁ = 45pF	19	22	ns
t _{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A ₀ to A ₇ = 2.4V, T/R = 2.4V (Figure 3) S ₃ = 1, R ₅ = 1k, C ₄ = 15pF	23	26	ns
t _{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A ₀ to A ₇ = 0.4V, T/R = 2.4V (Figure 3) S ₃ = 0, R ₅ = 1k, C ₄ = 15pF	18	21	ns
t _{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A ₀ to A ₇ = 2.4V, T/R = 2.4V (Figure 3)	38	43	ns
		S ₃ = 1, R ₅ = 100Ω, C ₄ = 300pF S ₃ = 1, R ₅ = 667Ω, C ₄ = 45pF	26	30	ns
t _{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A ₀ to A ₇ = 0.4V, T/R = 2.4V (Figure 3)	38	43	ns
		S ₃ = 0, R ₅ = 1k, C ₄ = 300pF S ₃ = 0, R ₅ = 5k, C ₄ = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t _{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/R to A Port	CD = 0.4V (Figure 2) S ₁ = 1, R ₄ = 100Ω, C ₃ = 5pF S ₂ = 1, R ₃ = 1k, C ₂ = 30pF	38	43	ns
t _{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/R to A Port	CD = 0.4V (Figure 2) S ₁ = 0, R ₄ = 100Ω, C ₃ = 5pF S ₂ = 0, R ₃ = 5k, C ₂ = 30pF	38	43	ns
t _{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/R to B Port	CD = 0.4V (Figure 2) S ₁ = 1, R ₄ = 100Ω, C ₃ = 300pF S ₂ = 1, R ₃ = 300Ω, C ₂ = 5pF	41	47	ns
t _{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/R to B Port	CD = 0.4V (Figure 2) S ₁ = 0, R ₄ = 1k, C ₃ = 300pF S ₂ = 0, R ₃ = 300Ω, C ₂ = 5pF	41	47	ns

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)
Am2947

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$CD = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$, $R_2 = 5\text{k}$, $C_1 = 30\text{pF}$	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$CD = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 1) $R_1 = 1\text{k}$, $R_2 = 5\text{k}$, $C_1 = 30\text{pF}$	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to $B_7 = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to $B_7 = 2.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to $B_7 = 0.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 1\text{k}$, $C_4 = 30\text{pF}$	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to $B_7 = 2.4\text{V}$, $T/\bar{R} = 0.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 5\text{k}$, $C_4 = 30\text{pF}$	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$CD = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$, $R_2 = 1\text{k}$, $C_1 = 300\text{pF}$	18	23	ns
		$R_1 = 667\Omega$, $R_2 = 5\text{k}$, $C_1 = 45\text{pF}$	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$CD = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 1) $R_1 = 100\Omega$, $R_2 = 1\text{k}$, $C_1 = 300\text{pF}$	16	23	ns
		$R_1 = 667\Omega$, $R_2 = 5\text{k}$, $C_1 = 45\text{pF}$	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to $A_7 = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to $A_7 = 2.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 1\text{k}$, $C_4 = 15\text{pF}$	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to $A_7 = 0.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 1$, $R_5 = 100\Omega$, $C_4 = 300\text{pF}$	25	35	ns
		$R_3 = 1$, $R_5 = 667\Omega$, $C_1 = 45\text{pF}$	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to $A_7 = 2.4\text{V}$, $T/\bar{R} = 2.4\text{V}$ (Figure 3) $S_3 = 0$, $R_5 = 1\text{k}$, $C_4 = 300\text{pF}$	26	35	ns
		$S_3 = 0$, $R_5 = 5\text{k}$, $C_1 = 45\text{pF}$	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/\bar{R} to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$, $R_4 = 100\Omega$, $C_3 = 5\text{pF}$ $S_2 = 1$, $R_3 = 1\text{k}$, $C_2 = 30\text{pF}$	28	38	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/\bar{R} to A Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$, $R_4 = 100\Omega$, $C_3 = 5\text{pF}$ $S_2 = 0$, $R_3 = 5\text{k}$, $C_2 = 30\text{pF}$	28	38	ns
t_{RTL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/\bar{R} to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 1$, $R_4 = 100\Omega$, $C_3 = 300\text{pF}$ $S_2 = 0$, $R_3 = 300\Omega$, $C_2 = 5\text{pF}$	31	40	ns
t_{RTH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/\bar{R} to B Port	$CD = 0.4\text{V}$ (Figure 2) $S_1 = 0$, $R_4 = 1\text{k}$, $C_3 = 300\text{pF}$ $S_2 = 1$, $R_3 = 300\Omega$, $C_2 = 5\text{pF}$	31	40	ns

Note: 1. All typical values given are for $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
 2. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
Am2947

Parameter	Description	Test Conditions	COMMERCIAL	MILITARY	Units
			Am2947	Am2947	
			Max	Max	
A PORT DATA/MODE SPECIFICATIONS					
t _{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R ₁ = 1k, R ₂ = 5k, C ₁ = 30pF	21	24	ns
t _{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/R = 0.4V (Figure 1) R ₁ = 1k, R ₂ = 5k, C ₁ = 30pF	21	24	ns
t _{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B ₀ to B ₇ = 0.4V, T/R = 0.4V (Figure 3) S ₃ = 1, R ₅ = 1k, C ₄ = 15pF	18	21	ns
t _{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B ₀ to B ₇ = 2.4V, T/R = 0.4V (Figure 3) S ₃ = 0, R ₅ = 1k, C ₄ = 15pF	18	21	ns
t _{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B ₀ to B ₇ = 0.4V, T/R = 0.4V (Figure 3) S ₃ = 1, R ₅ = 1k, C ₄ = 30pF	28	33	ns
t _{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B ₀ to B ₇ = 2.4V, T/R = 0.4V (Figure 3) S ₃ = 0, R ₅ = 5k, C ₄ = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t _{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1) R ₁ = 100Ω, R ₂ = 1k, C ₁ = 300pF	28	34	ns
		R ₁ = 667Ω, R ₂ = 5k, C ₁ = 45pF	22	25	ns
t _{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/R = 2.4V (Figure 1) R ₁ = 100Ω, R ₂ = 1k, C ₁ = 300pF	28	34	ns
		R ₁ = 667Ω, R ₂ = 5k, C ₁ = 45pF	22	25	ns
t _{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A ₀ to A ₇ = 0.4V, T/R = 2.4V (Figure 3) S ₃ = 1, R ₅ = 1k, C ₄ = 15pF	23	26	ns
t _{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A ₀ to A ₇ = 2.4V, T/R = 2.4V (Figure 3) S ₃ = 0, R ₅ = 1k, C ₄ = 15pF	18	21	ns
t _{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A ₀ to A ₇ = 0.4V, T/R = 2.4V (Figure 3) S ₃ = 1, R ₅ = 100Ω, C ₄ = 300pF	38	43	ns
		S ₃ = 1, R ₅ = 667Ω, C ₄ = 45pF	26	30	ns
t _{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A ₀ to A ₇ = 2.4V, T/R = 2.4V (Figure 3) S ₃ = 0, R ₅ = 1k, C ₄ = 300pF	38	43	ns
		S ₃ = 0, R ₅ = 5k, C ₄ = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t _{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/R to A Port	CD = 0.4V (Figure 2) S ₁ = 0, R ₄ = 100Ω, C ₃ = 5pF S ₂ = 1, R ₃ = 1k, C ₂ = 30pF	42	48	ns
t _{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/R to A Port	CD = 0.4V (Figure 2) S ₁ = 1, R ₄ = 100Ω, C ₃ = 5pF S ₂ = 0, R ₃ = 5k, C ₂ = 30pF	42	48	ns
t _{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/R to B Port	CD = 0.4V (Figure 2) S ₁ = 1, R ₄ = 100Ω, C ₃ = 300pF S ₂ = 1, R ₃ = 300Ω, C ₂ = 5pF	45	51	ns
t _{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/R to B Port	CD = 0.4V (Figure 2) S ₁ = 0, R ₄ = 1k, C ₃ = 300pF S ₂ = 1, R ₃ = 300Ω, C ₂ = 5pF	45	51	ns

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